



**NSAI**  
Standards

Irish Standard  
I.S. EN IEC 62878-2-5:2019

# Device embedding assembly technology - Part 2-5: Guidelines - Implementation of a 3D data format for device embedded substrate

**I.S. EN IEC 62878-2-5:2019**

*Incorporating amendments/corrigenda/National Annexes issued since publication:*

The National Standards Authority of Ireland (NSAI) produces the following categories of formal documents:

I.S. xxx: Irish Standard — national specification based on the consensus of an expert panel and subject to public consultation.

S.R. xxx: Standard Recommendation — recommendation based on the consensus of an expert panel and subject to public consultation.

SWiFT xxx: A rapidly developed recommendatory document based on the consensus of the participants of an NSAI workshop.

*This document replaces/revises/consolidates the NSAI adoption of the document(s) indicated on the CEN/CENELEC cover/Foreword and the following National document(s):*

*NOTE: The date of any NSAI previous adoption may not match the date of its original CEN/CENELEC document.*

*This document is based on:*

EN IEC 62878-2-5:2019

*Published:*

2019-11-08

*This document was published under the authority of the NSAI and comes into effect on:*

2019-11-25

ICS number:

NOTE: If blank see CEN/CENELEC cover page

NSAI  
1 Swift Square,  
Northwood, Santry  
Dublin 9

T +353 1 807 3800  
F +353 1 807 3838  
E standards@nsai.ie  
W NSAI.ie

Sales:  
T +353 1 857 6730  
F +353 1 857 6729  
W standards.ie

Údarás um Chaighdeán Náisiúnta na hÉireann

## National Foreword

I.S. EN IEC 62878-2-5:2019 is the adopted Irish version of the European Document EN IEC 62878-2-5:2019, Device embedding assembly technology - Part 2-5: Guidelines - Implementation of a 3D data format for device embedded substrate

This document does not purport to include all the necessary provisions of a contract. Users are responsible for its correct application.

For relationships with other publications refer to the NSAI web store.

**Compliance with this document does not of itself confer immunity from legal obligations.**

*In line with international standards practice the decimal point is shown as a comma (,) throughout this document.*

This page is intentionally left blank

EUROPEAN STANDARD

**EN IEC 62878-2-5**

NORME EUROPÉENNE

EUROPÄISCHE NORM

November 2019

---

ICS 31.180; 31.190

English Version

**Device embedding assembly technology - Part 2-5: Guidelines -  
Implementation of a 3D data format for device embedded  
substrate  
(IEC 62878-2-5:2019)**

Techniques d'assemblage avec intégration d'appareils -  
Partie 2-5 : Lignes directrices - Mise en œuvre d'un format  
de données 3D pour un substrat avec appareils intégrés  
(IEC 62878-2-5:2019)

Montageverfahren für eingebettete Bauteile - Teil 2-5:  
Implementierung eines 3D-Datenformats für Trägermaterial  
mit eingebetteten Bauteilen  
(IEC 62878-2-5:2019)

This European Standard was approved by CENELEC on 2019-10-21. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Republic of North Macedonia, Romania, Serbia, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.



European Committee for Electrotechnical Standardization  
Comité Européen de Normalisation Electrotechnique  
Europäisches Komitee für Elektrotechnische Normung

**CEN-CENELEC Management Centre: Rue de la Science 23, B-1040 Brussels**

## **EN IEC 62878-2-5:2019 (E)**

### **European foreword**

The text of document 91/1557/CDV, future edition 1 of IEC 62878-2-5, prepared by IEC/TC 91 "Electronics assembly technology" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 62878-2-5:2019.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2020-07-21
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2022-10-21

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC shall not be held responsible for identifying any or all such patent rights.

### **Endorsement notice**

The text of the International Standard IEC 62878-2-5:2019 was approved by CENELEC as a European Standard without any modification.



**IEC 62878-2-5**

Edition 1.0 2019-09

# **INTERNATIONAL STANDARD**



---

**Device embedding assembly technology –  
Part 2-5: Guidelines – Implementation of a 3D data format for device embedded  
substrate**





**THIS PUBLICATION IS COPYRIGHT PROTECTED**

**Copyright © 2019 IEC, Geneva, Switzerland**

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from either IEC or IEC's member National Committee in the country of the requester. If you have any questions about IEC copyright or have an enquiry about obtaining additional rights to this publication, please contact the address below or your local IEC member National Committee for further information.

IEC Central Office  
3, rue de Varembe  
CH-1211 Geneva 20  
Switzerland

Tel.: +41 22 919 02 11  
[info@iec.ch](mailto:info@iec.ch)  
[www.iec.ch](http://www.iec.ch)

**About the IEC**

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

**About IEC publications**

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigendum or an amendment might have been published.

**IEC publications search - [webstore.iec.ch/advsearchform](http://webstore.iec.ch/advsearchform)**

The advanced search enables to find IEC publications by a variety of criteria (reference number, text, technical committee,...). It also gives information on projects, replaced and withdrawn publications.

**IEC Just Published - [webstore.iec.ch/justpublished](http://webstore.iec.ch/justpublished)**

Stay up to date on all new IEC publications. Just Published details all new publications released. Available online and once a month by email.

**IEC Customer Service Centre - [webstore.iec.ch/csc](http://webstore.iec.ch/csc)**

If you wish to give us your feedback on this publication or need further assistance, please contact the Customer Service Centre: [sales@iec.ch](mailto:sales@iec.ch).

**Electropedia - [www.electropedia.org](http://www.electropedia.org)**

The world's leading online dictionary on electrotechnology, containing more than 22 000 terminological entries in English and French, with equivalent terms in 16 additional languages. Also known as the International Electrotechnical Vocabulary (IEV) online.

**IEC Glossary - [std.iec.ch/glossary](http://std.iec.ch/glossary)**

67 000 electrotechnical terminology entries in English and French extracted from the Terms and Definitions clause of IEC publications issued since 2002. Some entries have been collected from earlier publications of IEC TC 37, 77, 86 and CISPR.





**IEC 62878-2-5**

Edition 1.0 2019-09

# **INTERNATIONAL STANDARD**



---

**Device embedding assembly technology –  
Part 2-5: Guidelines – Implementation of a 3D data format for device embedded  
substrate**

INTERNATIONAL  
ELECTROTECHNICAL  
COMMISSION

---

ICS 31.180; 31.190

ISBN 978-2-8322-7399-9

**Warning! Make sure that you obtained this publication from an authorized distributor.**

## CONTENTS

FOREWORD.....	5
1 Scope.....	7
2 Normative references .....	7
3 Terms and definitions .....	7
4 Data definition .....	10
4.1 Flow chart design of device embedded substrate .....	10
4.2 Applicable range.....	11
4.2.1 Product.....	11
4.2.2 Process .....	12
4.3 Features .....	13
4.3.1 General .....	13
4.3.2 Device embedded substrate structure .....	13
4.3.3 SiP interposer structure .....	14
4.3.4 Virtual layer description .....	15
4.3.5 Terminal structure and embedded device structure including an SiP.....	15
4.3.6 Total design data of an SiP and device embedded substrate .....	15
4.4 Data description summary.....	16
4.4.1 Type of data and structures .....	16
4.4.2 File structure .....	18
4.5 3D expression.....	19
4.5.1 General .....	19
4.5.2 Coordinates.....	19
4.5.3 Position description .....	20
4.5.4 Relation between coordinate origin and board position .....	20
4.6 Layer concept .....	21
4.7 Substrate data .....	21
4.7.1 General .....	21
4.7.2 Layer map information .....	22
4.7.3 Device arrangement information .....	23
4.7.4 Basic figures.....	25
4.7.5 Net information .....	31
4.7.6 Artwork information.....	32
4.7.7 Package information .....	32
4.7.8 External port information.....	33
4.7.9 Internal port information.....	33
4.7.10 User expansion information .....	33
4.8 Defined data .....	33
4.8.1 General .....	33
4.8.2 Layer definition.....	33
4.8.3 Land definition.....	34
4.8.4 Via definition .....	35
4.8.5 Device definition .....	36
4.8.6 User expansion definition .....	37
5 Data organization and data description based on XML schema.....	38
5.1 General.....	38
5.2 Data organization of Example 1 .....	38
5.3 Data description of layer stack-up .....	39

5.4	Data description of device .....	43
5.5	Data organization of layer .....	47
5.6	Data description of via .....	50
5.7	Data description of land .....	51
	Bibliography .....	53
Figure 1	– Flow chart of design of device embedded substrate .....	11
Figure 2	– General structure of device embedded substrate .....	12
Figure 3	– Example of device embedded substrate structure .....	14
Figure 4	– Examples of SiPs .....	14
Figure 5	– Example of virtual layer description .....	15
Figure 6	– Terminal structure .....	15
Figure 7	– Structure of SiP on a device embedded substrate .....	16
Figure 8	– Data structure .....	18
Figure 9	– One file structure (recommended) .....	19
Figure 10	– Two file structure .....	19
Figure 11	– Definition of coordinates .....	20
Figure 12	– Position definition .....	20
Figure 13	– Relation between coordinates and board position .....	21
Figure 14	– Layer concept .....	21
Figure 15	– Layer construction .....	22
Figure 16	– Simplified layer construction .....	23
Figure 17	– Layer definition of pad connection .....	24
Figure 18	– Layer definition of via connection .....	24
Figure 19	– Rotation direction on <i>X</i> , <i>Y</i> , and <i>Z</i> axes .....	25
Figure 20	– Point .....	26
Figure 21	– Area .....	27
Figure 22	– Lines .....	27
Figure 23	– Letters .....	28
Figure 24	– Letter shape .....	28
Figure 25	– Bonding wire information .....	29
Figure 26	– Semi-sphere .....	29
Figure 27	– Truncated pyramid .....	30
Figure 28	– Via .....	30
Figure 29	– Device definition .....	31
Figure 30	– Group .....	31
Figure 31	– Data structure of net information .....	32
Figure 32	– Relation of layer definition data .....	34
Figure 33	– Land definition .....	35
Figure 34	– Relation between hole information and land information .....	36
Figure 35	– Device with internal connection information .....	37
Figure 36	– Device without internal connection information .....	37
Figure 37	– Cross sectional view of Example 1 .....	38
Figure 38	– Data organization of Example 1 .....	38

Figure 39 – Data description of Example 1 .....	39
Figure 40 – Layer structure of Example 1 .....	40
Figure 41 – Data description of layer stack-up .....	42
Figure 42 – Configuration of device 1 .....	43
Figure 43 – Data description of device 1 .....	44
Figure 44 – Configuration of device 2 .....	45
Figure 45 – Data description of device 2 .....	46
Figure 46 – Layer view of Example 1 .....	48
Figure 47 – Data description of layers .....	50
Figure 48 – Type of vias .....	51
Figure 49 – Data description of vias .....	51
Figure 50 – Type of lands .....	52
Figure 51 – Data description of lands .....	52
Table 1 – Required information .....	13
Table 2 – List of data .....	17

## INTERNATIONAL ELECTROTECHNICAL COMMISSION

---

### **DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –**

### **Part 2-5: Guidelines – Implementation of a 3D data format for device embedded substrate**

#### FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 62878-2-5 has been prepared by IEC technical committee 91: Electronics assembly technology.

This first edition cancels and replaces IEC PAS 62878-2-5 published in 2015. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

- a) the title has been changed to "Implementation of a 3D data format for device embedded substrate" from "Requirements of design data format for device embedded substrate";
- b) the scope of this implementation has changed to not include SiPs.

The text of this International Standard is based on the following documents:

CDV	Report on voting
91/1557/CDV	91/1589/RVC

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62878 series, published under the general title *Device embedding assembly technology*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

**IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.**

## DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

### Part 2-5: Guidelines – Implementation of a 3D data format for device embedded substrate

#### 1 Scope

This part of IEC 62878 specifies requirements based on XML schema that represents a design data format for device embedded substrate, which is a board comprising embedded active and passive devices whose electrical connections are made by means of a via, electroplating, conductive paste or printing of conductive material.

This data format is to be used for simulation (e.g. stress, thermal, EMC), tooling, manufacturing, assembly, and inspection requirements. Furthermore, the data format is used for transferring information among printed board designers, printed board simulation engineer, manufacturers, and assemblers.

This part of IEC 62878 applies to substrates using organic material. It neither applies to the re-distribution layer (RDL) nor to the electronic modules defined as M-type business model in IEC 62421.

#### 2 Normative references

There are no normative references in this document.

#### 3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

##### 3.1

###### **artwork information**

information that shows a SiP not included in net and figure data in board (symbol mark, inside of SiP, mould, spacer, remarks, etc.)

##### 3.2

###### **board information**

total information of a device-embedded substrate, including embedded devices

##### 3.3

###### **chip stack**

package of semiconductor chips stacked vertically

##### 3.4

###### **clearance**

area around a through-hole where there is no conductor to prevent electrical connection between a large conductor area, such as that of a power supply or a ground and a plated through-hole

This is a free preview. Purchase the entire publication at the link below:

[Product Page](#)

- 
- [Looking for additional Standards? Visit Intertek Inform Infostore](#)
  - [Learn about LexConnect, All Jurisdictions, Standards referenced in Australian legislation](#)
-