National Standards Authority of Ireland

IRISH STANDARD

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COMMON INTERFACE SPECIFICATION FOR CONDITIONAL ACCESS AND OTHER DIGITAL VIDEO BROADCASTING DECODER APPLICATIONS

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Údarás um Chaighdeáin Náisiúnta na hÉireann

DECLARATION

OF

SPECIFICATION

ENTITLED

COMMON INTERFACE SPECIFICATION FOR CONDITIONAL ACCESS AND OTHER DIGITAL VIDEO BROADCASTING DECODER APPLICATIONS

AS

THE IRISH STANDARD SPECIFICATION FOR

COMMON INTERFACE SPECIFICATION FOR CONDITIONAL ACCESS AND OTHER DIGITAL VIDEO BROADCASTING DECODER APPLICATIONS

NSAI in exercise of the power conferred by section 16 (3) of the National Standards Authority of Ireland Act, 1966 (No. 28 of 1996) and with the consent of the Minister for Enterprise, Trade and Employment, hereby declares as follows:

1. This instrument may be cited as the Standard Specification (Common interface specification for conditional access and other digital video broadcasting decoder applications) Declaration,1998.

2. (1) The Specification set forth in the schedule to this declaration is hereby declared to be the standard specification for Common interface specification for conditional access and other digital video broadcasting decoder applications. The Schedule comprises the text of EN 50221:1997.

(2) The said standard specification may be cited as Irish Standard EN 50221:1998 or as I.S. EN 50221:1998.

CENELEC

Corrigendum to EN 50221:1997

English version

NOTE The replacement (sub)clauses in this corrigendum correct an error in the PC Card metaformat information and adapt the text of EN 50221:1997 to accord with universal industry practice on the use of interrupts for module I/O.

Subclause 5.4.2, **replace** by:

5.4.2 Data and Command Logical Connections

The Physical Layer shall support independent both-way logical connections for the Transport Stream and for commands.
The Transport Stream Interface shall accept an MPEG-2 Transport Stream, consisting of a sequence of Transport Packets, either contiguously or separated by null data. The returned Transport Stream may have some of the incoming transport packets returned in a descrambled form. The Transport Stream Interface is subject to the following restrictions:

1 When the module is the source of a transport stream its output shall comply with ISO/IEC 13818-9.

2 Each output packet shall be contiguous if the module is the source of the packet or the input packet is contiguous.

3 A module shall introduce a constant delay when processing an input transport packet, with a maximum delay variation (tmdv) applied to any byte given by the following formula:

$$tmdv_{max} = (n * TMCLKI) + (2 * TMCLKO).$$

and

$$tmdv_{max} = 1 \text{ microsecond when } n = 0$$

where:

tmdv = Module Delay Variation
n = Number of gaps present within the corresponding input transport packet
TMCLKI = Input data clock period
TMCLKO = Output data clock period

* A 'gap' is defined to be one MCLKI rising edge for which the MIVAL signal is inactive. A 'gap' is always one byte width. Several 'gaps' may be contiguous.
* All hosts are strongly recommended to output contiguous transport packets.
* Hosts may only output non-contiguous transport packets if they implement less than 3 common interface sockets.
* Number of 'inter packet gaps' may vary considerably.

4 A CI compliant host should be designed to support Nm modules. Nm is the greater of the number of CI sockets implemented by the host or 16. It should tolerate the jitter resulting from Nm modules plus the jitter in the input transport stream. The worst case jitter may arise either from the host's own input followed by Nm modules or an input module with a ISO/IEC 13818-9 compliant output followed by (Nm - 1) modules.

5 All interfaces shall support a data rate of at least 58 Mb/s averaged over the period between the sync bytes of successive transport packets.

6 All interfaces shall support a minimum byte transfer clock period of 110 ns.

The Command Interface shall transfer commands as defined by the appropriate Transport Layer part of this specification in both directions. The data rate supported in each direction shall be at least 3,5 Megabits/sec.

Annex A, subclause A.2.2.1, **replace** by:

A.2.2.1 Hardware interface description

The hardware interface consists of several registers occupying 4 bytes of address space on the PC Card interface. Byte offset 0 is the Data Register. This is read to transfer data from the module and written to transfer data to the module. At byte offset 1 are the Control Register and Status Register. Reading at offset 1 reads the Status Register, and writing at offset 1 writes to the Control Register. The Size Register is a 16-bit register at byte offsets 2 and 3. Offset 2 is the Least Significant half and offset 3 the Most Significant half. The register map is shown in figure A.2.

Only two address lines, A0 and A1, are decoded by the interface. The host designer is free to place this block of 4 bytes anywhere within his own address space by suitable decoding or mapping of other address lines within the host.

Offset	Register
0	Data Register
1	Command/Status Register
2	Size Register (LS)
3	Size Register (MS)

Figure A.2: Map of Hardware Interface Registers

The Status Register looks like this:

bit	7	6	5	4	3	2	1	0
	DA	FR	R	R	R	R	WE	RE

DA (Data Available) is set to '1' when the module has some data to send to the host.
FR (Free) is set to '1' when the module is free to accept data from the host, and at the conclusion of a Reset cycle initiated by either a module hardware reset, or by the RS command..
R indicates reserved bits. They read as zero.
WE (Write Error) and RE (Read Error) are used to indicate length errors in read or write operations.

The DA and FR signals can also generate interrupts, controlled by Interrupt Enable bits in the Command Register.

The Command Register looks like this:

bit	7	6	5	4	3	2	1	0
	DAIE	FRIE	R	R	RS	SR	SW	HC

DAIE is set to '1' to enable the DA signal to assert the IREQ# signal on the PC card interface.
FRIE is set to '1' to enable the FR signal to assert the IREQ# signal on the PC card interface.
RS (Reset) is set to '1' to reset the interface. It does not reset the whole module.
SR (Size Read) is set to '1' to ask the module to provide its maximum buffer size. It is reset to '0' by the host after the data transfer.
SW (Size Write) is set to '1' to tell the module what buffer size to use. It is reset to '0' by the host after the data transfer.
HC (Host Control) is set to '1' by the host before starting a data write sequence. It is reset to '0' by the host after the data transfer.
R indicates reserved bits. They shall always be written as zero.