Irish Standard
I.S. EN 60191-6-17:2011

Mechanical standardization of semiconductor devices -- Part 6-17: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for stacked packages - Fine-pitch ball grid array and fine-pitch land grid array (P-PFBGA and P-PFLGA) (IEC 60191-6-17:2011 (EQV))

I.S. EN 60191-6-17:2011

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NSAI
1 Swift Square,
Northwood, Santry
Dublin 9

T +353 1 807 3800
F +353 1 807 3838
E standards@nsai.ie

W NSAI.ie

Sales:
T +353 1 857 6730
F +353 1 857 6729
W standards.ie

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EUROPEAN STANDARD

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EN 60191-6-17

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English version

Mechanical standardization of semiconductor devices - Part 6-17: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for stacked packages - Fine-pitch ball grid array and fine-pitch land grid array (P-PFBGA and P-PFLGA)

(IEC 60191-6-17:2011)

Normalisation mécanique des dispositifs à semiconducteurs -
Partie 6-17: Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs à montage en surface -
Guide de conception pour les boîtiers emplilés -
Boîtiers matriciels à billes et à pas fins et boîtiers matriciels à zone de contact plate et à pas fins (P-PFBGA et P-PFLGA)
(CEI 60191-6-17:2011)

Mechanische Normung von Halbleiterbauelementen -
Teil 6-17: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen -
Konstruktionsleitfaden für gestapelte Gehäuse -
Feinraster-Ball-Grid-Array und Feinraster-Land-Grid-Array (P-PFBGA/P-PFLGA)
(IEC 60191-6-17:2011)

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Management Centre: Avenue Marnix 17, B - 1000 Brussels

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Foreword

The text of document 47D/785/FDIS, future edition 1 of IEC 60191-6-17, prepared by SC 47D, Mechanical standardization for semiconductor devices, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60191-6-17 on 2011-03-03.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN and CENELEC shall not be held responsible for identifying any or all such patent rights.

The following dates were fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2011-12-03
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2014-03-03

Annex ZA has been added by CENELEC.

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Endorsement notice

The text of the International Standard IEC 60191-6-17:2011 was approved by CENELEC as a European Standard without any modification.

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Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

Publication	Year	Title	EN/HD	Year
IEC 60191-6	-	Mechanical standardization of semiconductor devices - Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages	EN 60191-6	-
IEC 60191-6-5	-	Mechanical standardization of semiconductor devices - Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for fine-pitch ball grid array (FBGA)	EN 60191-6-5	-

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

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FOREWORD

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International Standard IEC 60191-6-17 has been prepared by subcommittee 47D: Mechanical standardization for semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/785/FDIS	47D/793/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 60191 series, under the general title *Mechanical standardization of semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

The trend toward downsizing and higher density of portable electronic devices has driven LSI packages into smaller and higher density configurations. The market demand of higher density has led to the development of the package stacking technology that enabled miniaturization and higher functionality. The objective of this design guide is to standardize outlines and to get interchangeability of individual stackable packages.