



Irish Standard
I.S. EN 60191-6-22:2013

Mechanical standardization of semiconductor devices -- Part 6-22: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for semiconductor packages Silicon Fine-pitch Ball Grid Array and Silicon Fine-pitch Land Grid Array (S-FBGA and S-FLGA) (IEC 60191-6-22:2012 (EQV))

I.S. EN 60191-6-22:2013

Incorporating amendments/corrigenda issued since publication:

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EUROPEAN STANDARD
NORME EUROPÉENNE
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EN 60191-6-22

March 2013

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English version

**Mechanical standardization of semiconductor devices -
Part 6-22: General rules for the preparation of outline drawings of surface
mounted semiconductor device packages -
Design guide for semiconductor packages Silicon Fine-pitch Ball Grid
Array and Silicon Fine-pitch Land Grid Array (S-FBGA and S-FLGA)
(IEC 60191-6-22:2012)**

Normalisation mécanique des dispositifs à
semiconducteurs -
Partie 6-22: Règles générales pour la
préparation des dessins d'encombrement
des dispositifs à semiconducteurs à
montage en surface -
Guide de conception pour les boîtiers
matriciels à billes et à pas fins en silicium
et boîtiers matriciels à zone de contact
plate et à pas fins en silicium
(S-FBGA et S-FLGA)
(CEI 60191-6-22:2012)

Mechanische Normung von
Halbleiterbauelementen -
Teil 6-22: Allgemeine Regeln für die
Erstellung von Gehäusezeichnungen von
SMD-Halbleitergehäusen -
Konstruktionsleitfaden für
Halbleitergehäuse Si-Feinraster-Ball-Grid-
Array und Si-Feinraster-Land-Grid-Array
(S-FBGA und S-FLGA)
(IEC 60191-6-22:2012)

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Management Centre: Avenue Marnix 17, B - 1000 Brussels

Foreword

The text of document 47D/812/CDV, future edition 1 of IEC 60191-6-22, prepared by SC 47D, "Semiconductor packaging", of IEC TC 47, "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 60191-6-22:2013.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2013-10-15
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2016-01-15

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In the official version, for Bibliography, the following notes have to be added for the standards indicated:

| | | |
|----------------|------|------------------------------|
| IEC 60191-6 | NOTE | Harmonized as EN 60191-6. |
| IEC 60191-6-5 | NOTE | Harmonized as EN 60191-6-5. |
| IEC 60191-6-12 | NOTE | Harmonized as EN 60191-6-12. |

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

**Part 6-22: General rules for the preparation of outline drawings
of surface mounted semiconductor device packages –
Design guide for semiconductor packages Silicon Fine-pitch Ball Grid
Array and Silicon Fine-pitch Land Grid Array (S-FBGA and S-FLGA)**

FOREWORD

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International Standard IEC 60191-6-22 has been prepared by subcommittee 47D: Semiconductor packaging, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

| | |
|-------------|------------------|
| CDV | Report on voting |
| 47D/812/CDV | 47D/820/RVC |

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 60191 series, under the general title *Mechanical standardization of semiconductor devices*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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1 Scope

This part of IEC 60191 provides the outline drawings and dimensions common to silicon-based package structures and materials of ball grid array packages (BGA) and land grid array packages (LGA).

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

Void

3 Terms and definitions

For the purpose of this document, the following terms and definitions apply.

3.1

S-FBGA

FBGA composed of silicon die, dielectric layer(s) on the die, rerouting wires from the die pads to outer balls on the dielectric layer(s), and outer balls with heights more than 0,1 mm

3.2

S-FLGA

FLGA composed of silicon die, dielectric layer(s) on the die, rerouting wires from the die pads to outer lands on the dielectric layer(s), and outer lands with heights of 0,1 mm or less

4 Terminal position numbering

When a package is viewed from the terminal side with the index corner in the bottom left corner position, terminal rows are lettered from bottom to top starting with A, then B, C..., AA, AB, etc., whereas terminal columns are numbered from left to right starting with 1. Terminal positions are designated by a row-column grid system and shown as alphanumeric identification, e.g., A1, B1.

The letters I, O, Q, S, X and Z shall not be used for naming the terminal rows.

5 Code of package nominal dimensions

A code of package nominal dimensions is defined as the combination of package width *E* and length *D* which are shown in the second decimal place in millimeter.

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